REMARKS

Claims 3, 5, 11-12, 14, 18-20, 25, and 27-30 have been canceled. Thus, claims 1-2, 4, 6-10, 13, 15-17, 21-24, 26, and 31-40 are pending in the present application.

In the Office Action, claims 25 and 26 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Claim 25 has been canceled, rendering the Examiner's rejection of this claim moot. With regard to claim 26, Applicant respectfully submits that support for the claim may be found at least at line 15-17 on page 47 of the specification. Thus, claim 26 complies with the written description requirement. Applicant requests that the Examiner's rejection of claim 26 under U.S.C. § 112, first paragraph, be withdrawn.

In the Office Action, claims 11 and 18 were rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claims 11 and 18 have been canceled, rendering the Examiner's rejections of these claims moot.

In the Office Action, claims 1-40 were rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Wells, et al (U.S. Patent No. 6,687,721). Claims 3, 5, 11-12, 14, 18-20, 25, and 27-30 have been canceled, rendering the Examiner's rejections of these claims moot. The Examiner's remaining rejections are respectfully traversed.

With regard to independent claims 1, 9, 22, 31, and 36, Applicant describes and claims, among other things, a random number generator that includes an entropy register configured to receive a plurality of bits from a corresponding plurality of performance registers. As defined in the specification, performance registers each store a value indicative of a different performance metric. Exemplary performance metrics may include first-level-cache hit rate, second-level-

cache hit rate, third-level-cache hit rate, branch target cache, and/or other model specific registers (MSRs), such as those used for measuring performance. In one embodiment, the performance registers include any register that updates the least significant bit at a rate asynchronous to the local and/or system clock. See Patent Application, page 46, l. 23 - page 47, l. 5.

In contrast, Wells describes an entropy accumulator that may receive one or more random number bits from one or more random bit sources 210. See Wells, Figures 2 and 7 and related discussion. The random bit sources 210 comprise circuitry for generating random bits. See Wells, col. 4, ll. 34-35 and Figure 4. However, Wells is completely silent with regard to performance registers. Thus, Wells does not teach or suggest a random number generator that includes an entropy register configured to receive a plurality of bits from a corresponding plurality of performance registers. For at least this reason, Applicant respectfully submits that the present invention is not anticipated by Wells and requests that the Examiner's rejections of claims 1-2, 4, 6-10, 13, 15-17, 21-24, 26, and 31-40 be withdrawn.

Moreover, it is respectfully submitted that the pending claims are not obvious in view of Wells. To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). As discussed above, Wells does not teach or suggest a random number generator that includes an entropy register configured to receive a plurality of bits from a corresponding plurality of performance registers. Wells also fails to provide any suggestion or motivation to modify the prior art to arrive at Applicant's claimed invention. To the contrary, Wells appears to teach away from Applicant's claimed invention. Wells teaches that random bits should be provided to the entropy register, which teaches away from providing bits related to one

or more performance metrics. It is by now well established that teaching away by the prior art constitutes *prima facie* evidence that the claimed invention is not obvious. *See, inter alia, In re Fine*, 5 U.S.P.Q.2d (BNA) 1596, 1599 (Fed. Cir. 1988); *In re Nielson*, 2 U.S.P.Q.2d (BNA) 1525, 1528 (Fed. Cir. 1987); *In re Hedges*, 228 U.S.P.Q. (BNA) 685, 687 (Fed. Cir. 1986).

For the aforementioned reasons, it is respectfully submitted that all claims pending in the present application are in condition for allowance. The Examiner is invited to contact the undersigned at (713) 934-4052 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

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